

WE CLAIM:

1 1. A data communication system for a semiconductor memory system having at
2 least one data path, the data communication system comprising:
3 a central data path including at least one junction circuit configured for
4 exchanging data signals between the central data path and at least one data path of the at least
5 one data path;
6 a respective one junction circuit of the at least one junction circuit including
7 means for controlling resetting the respective one junction circuit for preparation of a
8 subsequent data transfer through the respective one junction circuit in accordance with receipt
9 of an input monitor signal indicating that data has been transferred to the respective one
10 junction circuit.

1 2. The data communication system of Claim 1, wherein the means for controlling
2 resetting prevents resetting of the respective one junction circuit when data is being received
3 by the respective one junction circuit.

1 3. The data communication system of Claim 1, wherein the data communication
2 system includes a plurality of data banks configured for storing data, and a corresponding
3 data bank of the plurality of data banks is connected to a respective one data path of the at
4 least one data path, the data communication system including:
5 means for controlling the respective one data path in accordance with receipt
6 of a monitor signal indicating that a data transfer operation has been initiated for transfer of
7 data to the respective one data path, the means for controlling including a means for

1 generating a control signal for controlling resetting of the respective one data path after data
2 is transferred for preparation of a subsequent data transfer operation.

1 4. The data communication system of Claim 3, wherein the control signal is
2 provided to the means for generating the control signal as a feedback signal.

1 5. The data communication system of Claim 1, wherein the input monitor signal
2 indicates that a plurality of data signals are being transferred to the respective one junction
3 circuit, and wherein the respective one junction circuit outputs an output monitor signal
4 indicating that the plurality of data signals are being transferred from the respective one
5 junction circuit.

1 6. The data communication system of Claim 5, wherein the respective one
2 junction circuit includes a plurality of junction data lines for at least one of processing,
3 receiving and transferring at least one of the input monitor signal, the plurality of data signals,
4 and the output monitor signal.

1 7. The data communication system of Claim 6, wherein the plurality of
2 junction data lines includes a plurality of input data signal lines and at least one input monitor
3 signal line; and
4 wherein the respective one junction circuit receives the input monitor signal
5 via an input monitor signal line of the at least one input monitor signal line, and a plurality of

1 input data signals via a group of input data signal lines of the plurality of input data signal
2 lines.

1 8. The data communication system of Claim 6, wherein the respective
2 one junction circuit of the at least one junction circuit includes a plurality of output data
3 signal lines and at least one output monitor signal line; and
4 wherein the respective one junction circuit outputs an output monitor signal
5 via an output monitor signal line of the at least one output monitor signal line; and a plurality
6 of output data signals via the plurality of output data line.

1 9. The data communication system of Claim 7, wherein the means for controlling
2 resetting controls resetting of the input monitor signal line propagating the input monitor
3 signal and the group of input data signal lines propagating the plurality of input data signals.

1 10. The data communication system of Claim 7, wherein the respective
2 one junction circuit of the at least one junction circuit includes a plurality of output data
3 signal lines and at least one output monitor signal line;
4 wherein the respective one junction circuit outputs an output monitor signal
5 via an output monitor signal lines of the at least one output monitor signal line, and a plurality
6 of output data signals via a group of output data signal lines of the plurality of output data
7 signal lines; and
8 wherein the input monitor signal is received from one of a data path of the

1 plurality of data paths and the output monitor signal line of another junction circuit of the at
 2 least one junction circuit, and the plurality of input data signals is received from one of a data
 3 path of the plurality of data paths and the group of output data signal lines of the another
 4 junction circuit of the at least one junction circuit.

1 11. The data communication system of Claim 8, wherein the plurality of
 2 junction data lines includes a plurality of input data signal lines and at least one input monitor
 3 signal line;

4 wherein the respective one junction circuit receives the input monitor signal
 5 via an input monitor signal line of the at least one input monitor signal line, and a plurality of
 6 input data signals via a group of input data signal lines of the plurality of input data signal
 7 lines; and

8 wherein the output monitor signal is transmitted to [one of a data path of the
 9 plurality of data paths and] the input monitor signal line of another junction circuit of the at
 10 least one junction circuit, and the output data signals are transmitted to [one of a data path of
 11 the plurality of data paths and] the group of input data signal lines of the another junction
 12 circuit.

1 12. The data communication system of Claim 6, wherein the means for
 2 controlling resetting includes at least one reset circuit included in at least one of the plurality
 3 of junction data lines, and a control signal generator for generating a reset control signal
 4 which controls the at least one reset circuit.

1 13. The data communication system of Claim 6, wherein a respective junction
2 data line of the plurality of junction data lines is connected to a discharge circuit for
3 transferring at least one of the received input monitor signal and the plurality of data signals.

1 14. The data communication system of claim 13, wherein the at least one
2 discharge circuit includes a discharge device;
3 wherein the means for controlling resetting includes a control signal generator
4 for generating a reset control signal which controls resetting the respective one junction
5 circuit, and a virtual ground signal having a polarity different from the reset control signal;
6 and
7 wherein the virtual ground signal is applied to the discharge device.

1 15. The data communication system of Claim 12, wherein feedback
2 signals are provided to the control signal generator.

1 16. The data communication system of Claim 12, wherein the reset control signal
2 prevents resetting of the plurality of junction data lines when the plurality of data signals and
3 the input junction monitor signal are being received or processed by the junction data lines.

1 17. The data communication system of Claim 12, wherein the input monitor signal
2 is a pulse signal, and the reset control signal disables the at least one reset circuit for the
3 duration of a pulse of the input monitor signal.

1 18. The data communication system of Claim 12, wherein the reset circuit is a pre-
2 charge circuit.

1 19. The data communication system of Claim 12, wherein the reset
2 control signal is a pulse signal generated by a pulse generator.

1 20. The data communication system as in Claim 21, wherein the pulse generator is
2 triggered by a signal indicative of the input monitor signal.

1 21. A method for transferring data in a data communication system for a
2 semiconductor memory system having at least one data path comprising the steps of:
3 connecting a central data path to the at least one data path at a junction circuit;
4 receiving data in the junction circuit;
5 processing the data;
6 transferring the data out of the junction circuit;
7 resetting of the junction circuit for preparation for receipt of new data; and
8 controlling the resetting to prevent resetting while the data is being at least one
9 of received and processed.

1 22. The method of Claim 21, further including the steps of:
2 receiving an input monitor signal indicating that the data is being transferred
3 to the junction circuit; and

1 outputting an output monitor signal indicating that the data is being transferred
2 from the junction circuit.

1 23. The method of Claim 22, wherein the step of controlling further
2 includes the steps of:
3 generating a reset control signal in accordance with receipt of the input
4 monitor signal; and
5 controlling via the reset control signal at least one reset circuit associated with
6 data lines receiving data and the input monitor signal.

1 24. The method of Claim 23, further comprising the steps of generating the reset
2 control signal via a pulse generator; and
3 triggering the pulse generator by a signal indicative of the input monitor
4 signal.

1 25. A data communication system for a semiconductor memory system
2 having at least one data path, the data communication system comprising:
3 means for connecting a central data path to the at least one data path at a
4 junction circuit;
5 means for receiving data in the junction circuit;
6 means for processing the data;
7 means for transferring the data out of the junction circuit;

1 means for resetting the junction circuit for preparation of receipt of new
2 data; and
3 means for controlling the resetting to prevent resetting while the data is being
4 at least one of received and processed.

1 26. The data communication system of Claim 25, further comprising:
2 means for receiving an input monitor signal indicating that the data is being
3 transferred to the junction circuit; and
4 means for outputting an output monitor signal indicating that the data is being
5 transferred from the junction circuit.

1 27. The data communication system of Claim 26, wherein the means for
2 controlling further includes:
3 means for generating a reset control signal in accordance with receipt of the
4 input monitor signal; and
5 means for resetting including at least one reset circuit associated with data
6 lines receiving data and the input monitor signal controlled via the reset control signal.

1 28. The data communication system of Claim 27, wherein the reset
2 control signal is generated via a pulse generator, and further including means for triggering
3 the pulse generator by a signal indicative of the input monitor signal.